

Optical methods of the delay cells characteristics measurements and their applications

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Abstract The only efficient optical spectrum measurement in infra-red range for low light regime is based on time multiplexing. Typically low timing jitter of the single photon detector combined with fast and high precision electronics is used for photon arrival time measurement. The timing histogram can be used to determine the spectrum of the photons. The better time detection accuracy allows to obtain the more precise spectrum information. This paper proposed an optical method for the sub-picosecond time-to-digital converters characterization prefer to optimize the multi-tapped delay lines implementation process, thus yielding the converters with much improved parameters.

Keywords Optical delay line · Field programmable gate array · Time-interval measurement · Delay cells · Optical and quantum measurements

1 Introduction

Since last 10 years, many different techniques of using Tapped Delay Lines (TDL) to measure the sub-nanosecond time intervals has been used for the construction of various types the Time-to-Digital Converters (TDC) implemented in Field-Programmable-Gate-Array (FPGA) structures (Zielinski et al. 2004; Kalisz 2004).

The most of them has been widely used in different scientific experiments such as the life-time of excited atomic states measurements, the spectral state of single photon

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experimental characterization (Frankowski 2006; Wasilewski et al. 2007) and the time-flight measurements applied in the time-of-flight mass spectrometry, where an isotopic composition of the atomic beam is measured (Song et al. 2006; Zieliński et al. 2003). Furthermore, TDCs have been also employed in laser ranging systems, telecommunication systems (for skew measurements) and also in many other experiments which are useful in many field of quantum physics (Lutz et al. 2014) i.e. optical quantum information processing schemes, quantum cryptography protocols and quantum teleportation.

As long as, the precision of TDCs largely depends on quantization parameters, then it is necessary to seeking the new solutions aiming to increase the TDLs resolution and accuracy. Due to the rapid development of microelectronic technology and quick prototyping makes the new series of highest performance FPGAs as a very interesting solution for future investigations.

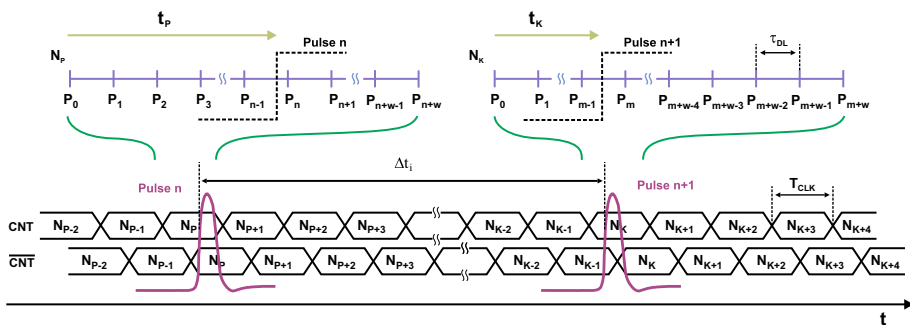
The new FPGAs generation provide (inside CMOS structure) an array of fast Configurable Logic Blocks (CLB) which constituent components such as: simple logic gates, four and more inputs Look-up Tables (LUT) and fast dual-edge D-type flip-flops (FF) are characterized by a very small propagation times. Its facilities provide the ability to implement in a suitably large structures the multi-stage tapped delay lines (MTDL) with picoseconds and sub-picosecond resolution (Zhang and Zhou 2015; Park et al. 2015). Implementation of such delay lines, requires a new characterization method for testing and calibration. The proposed in this article the optical delay line (ODL) meets these requirements.

This paper is organized as follows. At the beginning we analyze the TDC architectures (in Sect. 2) and explain the TDL process implementation (in Sect. 3). In Sects. 4 and 5 we present a new method for optical measuring of the delay line characteristics. Using this method, we obtain the distributions of probabilities of counts in each time-channels. This informations will be helpfull to determine the level and character of distribution random error which describing a direct coding delay line (TCDL) representing by high precision TDL and coding register module. For further improvement of a one-shot TCDL resolution and effectively minimization of the non-linearity errors we also implemented and characterized (in Sect. 6) an equivalent coding delay line (ECDL) (Szplet et al. 2013). Finally, we summarize our work and suggest possible directions for future investigations.

The presented studies will concern on implementation and characterization of TDLs in XC4VFX12 FPGAs device.

2 Flash-like TDC architecture

Usually, the heart of high-precision time-to-digital conversion are the phase measuring (PM) modules. Each of PM modules may contain one or more delay lines in many different configurations. For example, to improve of the TDCs resolution may be used an vernier (Zieliński et al. 2005), pulse shrinking (Zhang and Zhou 2015; Szplet and Klepacki 2010) and interpolation techniques (Jansson et al. 2006) where effective resolution depends on the difference between two various LEs propagation times. In other cases, for decrease a dead time and adaptation to multichannel solutions we apply a Flash-like architecture with direct coding lines (Ugur et al. 2012). Consequently, a wide spectrum of TDL architectures determines the most interesting TDCs parameters such as precision, resolution, dead time (the minimum time between two measurements), maximum pulses intensity and limiting the measurement range (the maximum time interval which can be measured).

$$\Delta t_i = (m - n)\tau_{DL} + (N_k - N_p)T_{CLK} \quad (1)$$
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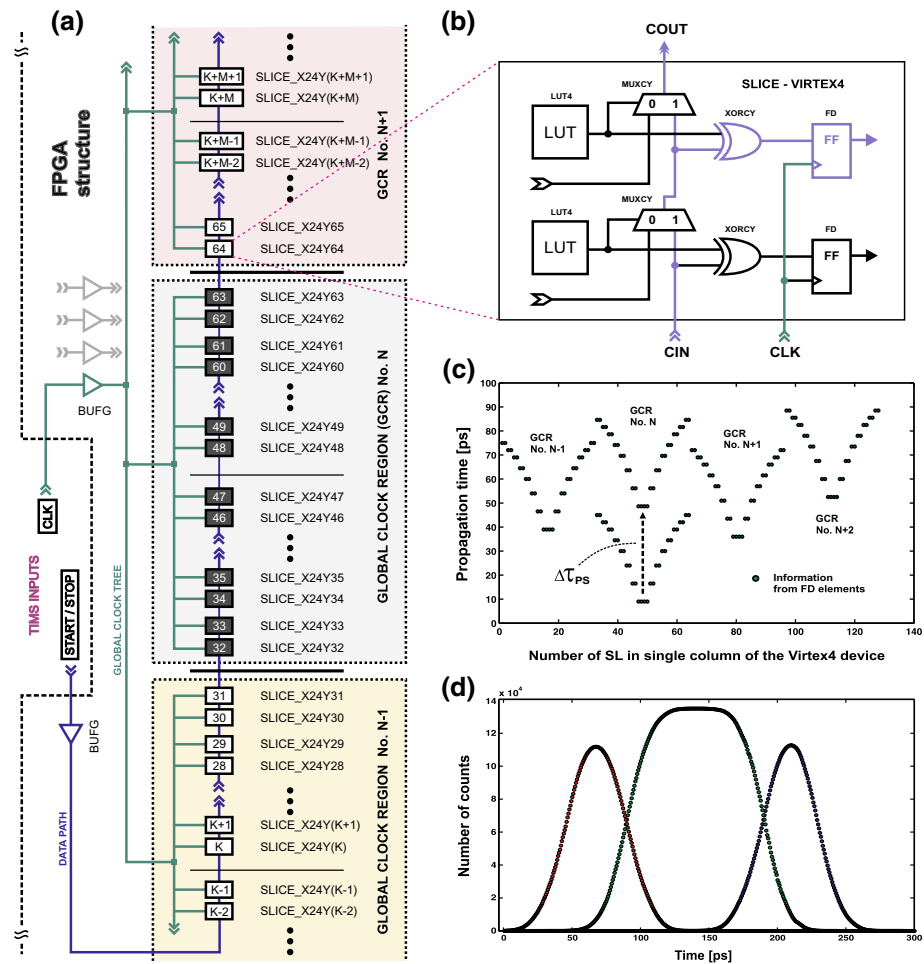


Fig. 2 The multi-tap delay lines implementation: **a** delay cells structure inside the part of single column of the FPGA XC4VFX12 device, **b** single delay cell architecture, **c** the propagation time from input global clock buffer to each of the delay cells, **d** delay cells characteristics

the global clock buffers can drive all clock regions. The used in this paper XC4VFX12 device contain sixteen GCIs and improve the clocking distribution by eight clock regions. Whereas, the main logic resources used for implementing sequential and combinational modules are realized in CLBs. Each of CLB elements contains four slices (SL) which are grouped in two pairs (two SL together) and may be connected to SMC matrix. Each pair is organized as a column using an independent fast carry chain interconnection. In Fig. 2a is shown only part of above single column without indicating the CLB blocks. Delay cells are often implemented with use the logical elements (LE), placed inside SLs and fast carry chain interconnections (Fig. 2b). Delays of that individual delay cells are usually about tens of picoseconds and depends on FPGA technology.

The main purpose of delay line implementation is to produce a multiphase clock signal and precise phase shifting. A common problem in the implementation process is to guarantee a linearity of the TCDL characteristics. In the real case, the non-linearity

problem concerns of differences in the data and clock propagation times. The maximum differences between propagation time to each of global clock regions are at the level of twenty picoseconds and depends on TCDL location in programmable structure. Other signal propagation times within regions are comparable. It should be noted, that all of these propagation times includes the FF setup time. The setup and propagation time disturbances may also cause in the random mistakes during the conversion process which may result in not pseudo-thermometric output code (presents some bubbles) (Frankowski 2011). Thus, it requires either a hardware and software correction.

The hardware calibration process of the delay line non-linearities may be realized in several ways. In the easiest form, it require by selecting the one of two available LE locations in single delay cell architecture (Fig. 2b). Another method involves attaching the input capacity (by connecting unused gates) to increase the propagation time of individual delay elements. The last way of hardware linearization applies an appropriate choice of the global clock buffer allocation that distributing the clock signal to the clock regions. Further correction can be achieved by the DCM module (signs in Fig. 2c as $\Delta\tau_{PS}$), running in a precision phase shifting configuration.

4 Optical direct method

A TDL time-resolution measurement was performed by optical system constructed in the National Laboratory for Atomic, Molecular and Optical Physics in Toruń, Poland. With them used, it was possible to perform the test pulses with a 40 ps timing jitter. An schematic of experiment setup designed to determine of the DCs characteristics and their practical realization are shown in Fig. 3. For this solution, precise change distance between two pulses may be realized through precision shifting of the retroreflector position. It was possible with used precision platform with ball screw and stepper motor, with step equal to 0.1 mm. Thus, the precision with which you can change the geometric light distance, determines the temporal resolution of an ODL. In the present case it is possible to precisely

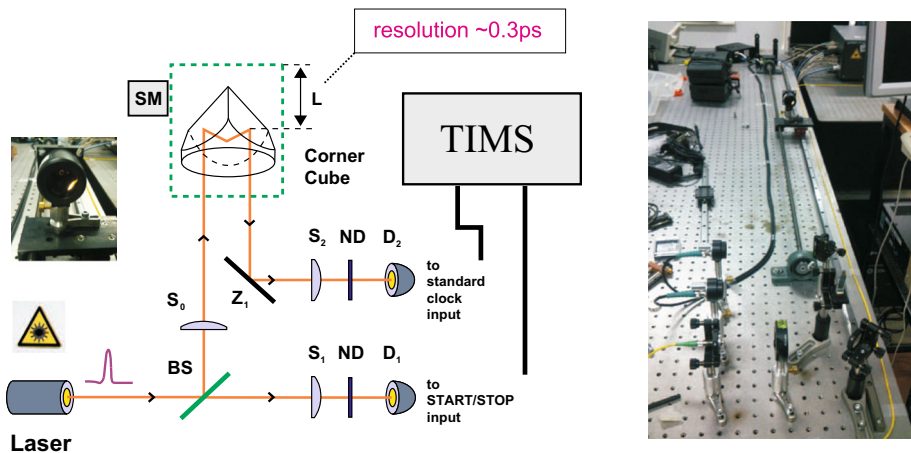


Fig. 3 The schematic setup of the experiment to determine the MTDL characteristics by the optical direct method. Description of designations: *BS* beam splitter, *CC* corner cube (retroreflector), *SM* stepper motor, *Z* mirror, *S* lens, *ND* neutral filter, *D1* and *D2* avalanche photodiodes id101 (idQuantique), *TIMS* time interval measurement system

delaying the signal with a resolution about 0.34 ps. Of course, it should be noticed, that it is also possible to increase the step resolution up to 50 μm . The nominal lead of used in the experiment a ball screw has 5 mm per revolution. Hence, the accuracy grade of lead error shall amount 50 μm . From a practical point of view, the stepper motor positioning accuracy (for stepper motor which has 200 steps per revolution) is about 5 % of its step. Therefore, the maximum error of positioning is calculated by sum of the lead error and the stepper motor error. The corresponding to him of the maximum delay error is about 0.18 ps (Fig. 4).

Experiments were performed with femtosecond laser system (Wave Pack, Warsaw University) that delivers 40 femtosecond pulses (FWHM) centered around 774 nm at about 80 MHz repetition rate. Transmitted beam through the retroreflector was collected fully onto a D_2 detector (avalanche photodiodes id101—idQuantique) using a lens. Neutral density filters were used to perform experiments on the same intensities of the light beam. In this way, the registered by the D_1 and D_2 detectors signals had similar characteristics.

5 Determination of delay cells characteristics

With proposed in Sect. 4 direct method it is possible to recreate the real characteristics of the delay line. Registered information obtained by this method provides detailed information about probabilities of counts for the each positions (number of positions depends on the ODL resolution) of the pulse inside the experimental time channel where it was qualified (shown in Fig. 4). Therefore, the probability distribution functions (for particular channels) may be strictly defined. Knowledge of such information allows to determining non-linearity parameters such as differential and integral nonlinearities (INL and DNL) and also parameters of envelope functions (EF) and then information about the TCDLs module random error distribution.

5.1 Distribution of random errors

Measurement of TDLs characteristics using an optical direct method assumes strong correlation between the signals propagated into delay line and registered information from the TDL in the registry. Therefore, performing K successive changes of the geometric light distance it was possible to collect the total number of counts for each of N time channels.

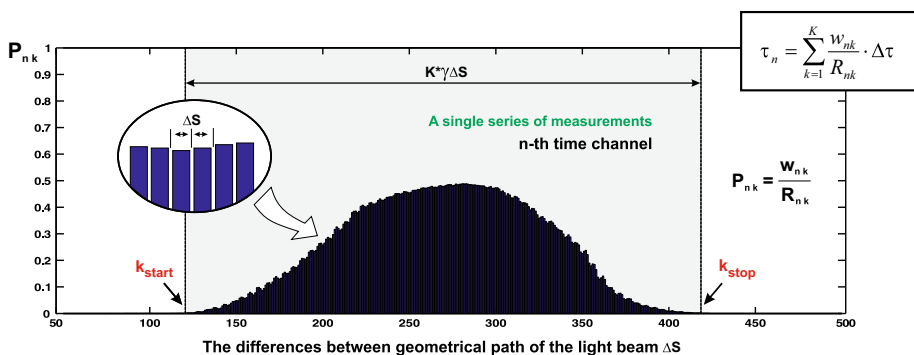


Fig. 4 Principle of the direct method—the probability of counts in the k -th sub-channel of n -th delay cell: ΔS —a minimal geometrical change of the light beam (the distance that light is present in a vacuum at a given time)

Based on the collected information can be determined the probability of counts in the k -th sub-channels contained in the n -th delay cell. Discrepancies between the collected (for each of DCs) probabilities of counts, depends on the TCDLs implementation architectures and allow us to designate the various specific for a given technology of the delay cells parameters. The greatest impact to this, have such factors as: the individual FF or LEs technological properties and the propagation times disturbances. Below we proposed a mathematical model describing the nature of this phenomenon, using for this purpose the cumulative distribution function (CDF) defined as:

$$F_i(t_i, \sigma_i) = \int_{-\infty}^x \Phi(t) dt \quad (2)$$

where Φ is the Gaussian standard normal probability density function (PDF) with standard deviation σ_i and mean t_p^i . Bearing in mind the need to transform it into a simpler form, (which is required for further computation) we can approximated the CDF by the *erf* function, as shown in next formula:

$$F_i(t_i, \sigma_i) = 2^{-1} \left\{ 1 + \operatorname{erf} \left(\frac{t - t_p^i}{\sigma_i \sqrt{2}} \right) \right\} \quad (3)$$

where the classical error function is defined by:

$$\operatorname{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x \exp(-t^2) dt \quad (4)$$

An important problem is that the error function has no analytical solution. Nevertheless, there are several solutions which provide an approximation of these functions by many of the numerical methods (Patel and Read 1996). Unfortunately, the numerical integration is more expensive in computation time. Therefore is not suitable solution for implementation these forms to quick computational calculations and real-time processing. However, it was possible to solve, approximate analytic solution for the cumulative normal distribution and error functions. For this purpose we given the simplicity formula which was proposed by Winitzki (2008).

The complementary of these analytical error function, (denoted in relation to the *erf* and *erfc* functions) is defined as:

$$A_i(t_i, \sigma_i) = 1 - F_i(t_i, \sigma_i) \quad (5)$$

From probability theory, a non-zero probability of counts in adjacent time channel depends on the probabilities of counts in the other time channels which are representing by another FF creating the next delay cells. Thus, the probability of these events is equal to the product of the probabilities and can be written in the following form:

$$\Gamma_i(t_i, \sigma_i, t_{i+n}, \sigma_{i+n}) = F_i(t_i, \sigma_i) \prod_{n=1}^N (1 - F_{i+n}(t_{i+n}, \sigma_{i+n})) \quad (6)$$

Assuming that the τ_{DL} resolution is much greater than 3σ the above formula can be reduce to their simplified form as follow:

$$\Gamma_i(t_i, \sigma_i, t_{i+1}, \sigma_{i+1}) = F_i(t_i, \sigma_i) A_{i+1}(t_{i+1}, \sigma_{i+1}) \quad (7)$$

Whereas, for the case of a delay line that meets the above assumption and consisting of two delay cells, we obtain the following two expressions:

$$\Gamma_1(t_1, \sigma_1, t_2, \sigma_2) = F_1(t_1, \sigma_1)A_2(t_2, \sigma_2) \quad (8)$$

$$\Gamma_2(t_2, \sigma_2, t_3, \sigma_3) = F_2(t_2, \sigma_2)A_3(t_3, \sigma_3) \quad (9)$$

The results of fitting Γ_i functions (named further as EF) for three randomly selected delay cells by used a least squares method are shown in Fig. 5. An EF can be determined for each of MTDL time channels. For this purpose each of the DL taps can be approximated by the CDF. In the real case, the EFs of individual delay cells may be describes by different number of CDF parameters (standard deviation, mean). This fact affect the large asymmetry of EFs. Using the above EFs will be possible to designating the appropriate PDF Θ_n through their normalization (Fig. 6). Knowledge of these functions allows to divide each of real MTDLs channel into multiple time sub-channels and preparation the two sample difference histogram with any finite resolution greater than TDC resolution (Frankowski and Zieliński 2015). Furthermore, knowledge of their coefficients will enable the determination of distribution random errors describing a high precision multi-tapped delay line with coding register module (Fig. 7).

5.2 Noise level analysis

The precision of a measurement is permanently limited by the random errors which usually may be determined by repeating the measurements. In most cases, the main sources of random errors are thermal noises and slope disturbances in the electronic circuits. In practice, the thermal noise is a white noise with a constant spectral density which is characterized by a Gaussian distribution of amplitude. Therefore, this random errors are often described by a Gaussian normal distribution parameters.

Consequence of noise or slope disturbances is jitter defined as phase fluctuations in a signals propagated inside the global clock and data path trees (Fig. 2a). The first one relates mainly to the delay cells architecture, while the second one to the global clock trees. Thus, the noise model of global clock path depends on differences in propagation times and can be approximated by:

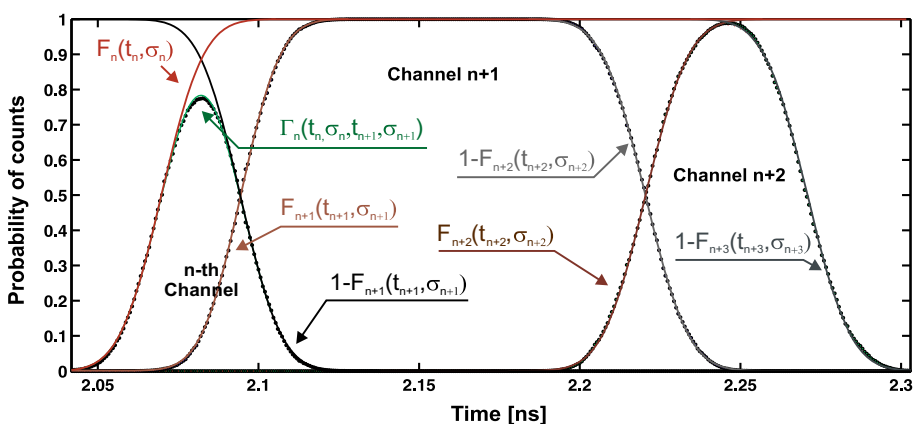


Fig. 5 Envelope functions $\Gamma_i(t, \sigma)$ creation as results of fitting F_i and $A_i = 1 - F_i$ functions performed for three randomly selected delay cells

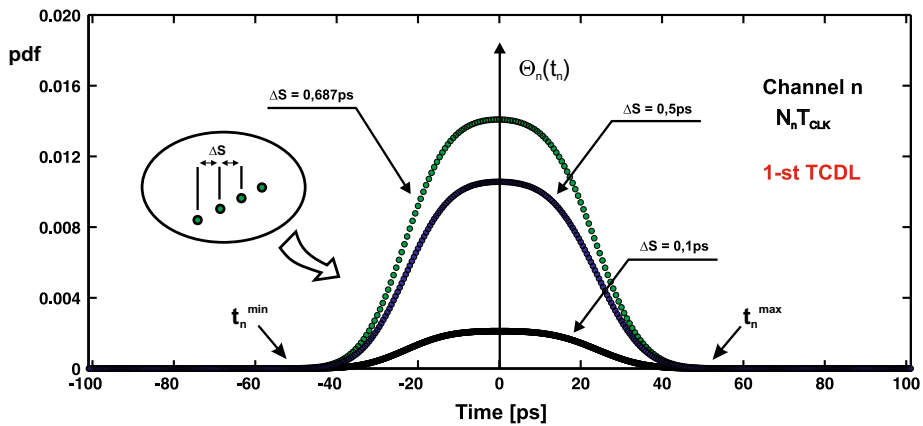


Fig. 6 Principle of the probability density functions creation

$$\sigma_{clk} \cong S^{-1} U_{max} \quad (10)$$

where: U_{max} is the peak amplitude of noise voltage, whereas S represents a signal slope. For a given bandwidth B , the root mean square (RMS) value of the noise voltage is given by:

$$U_{rms} = \sqrt{4kTBR} \quad (11)$$

where: k is the Boltzmann's constant, T is the absolute temperature of the resistive R component (in Kelvin degrees).

In order to determine the amplitude peak of the noise, we must designate the relevant parameters of noise such as rms and mean values. The peak-to-peak noise volts in a distributed signals depends on level of crest factor (CF) and noise rms value. Typically, the CF is unitless coefficient which can be used to describe the purity of voltage signal. In our applications has been defined as the ratio of the peak value to the rms value:

$$|U_{max} - U_0| = CF \cdot U_{rms} \quad (12)$$

From the selected CF we can predict the probability of an occurrence of noise peaks that exceeds the proposed voltage peak-to-peak limits. In most cases, the CF value is accepted at a sufficient level equal to 3.9. For such value an occurrences of exceeding peaks outside the CF limits will be 0.01. For this range the peak-to-peak noise volts in a inputs signals may be obtained from:

$$U_{p-p} = 2 \cdot CF \cdot U_{rms} \quad (13)$$

where: U_{rms} is the statistical standard deviation of the noise signal.

To characterize time jitter in the delay cells structure (data path tree) we must take into account the contributions of successive multiplexers, placed inside the slices. If we assume that the single stage of multiplexers to introduces a time-jitter given by σ_{MUX} and that jitter values for others multiplexers are uncorrelated, we can designate a formula that describe the n -th tap error:

$$\sigma_{data} = \sigma_{MUX} \sqrt{kn} \quad (14)$$

where: k —indicates the number of multiplexers which forming a single delay cell.

Presented phase fluctuations, are uncorrelated and described by Gaussian distribution $\Phi(t - \Delta t_p, \sigma)$ with standard deviation σ and centered at Δt_p . The experimental results of measurement the random errors disturbances for one-stage TCDL was shown in Fig. 7.

5.3 Differential and integral non-linearities

Performing K successive changes of the geometric light distance and collecting the total number of counts for each of N time channels it was possible to determine the delay cells characteristics for the whole delay line. According to this, the width of the n -th time channel can be described by the following formula:

$$\tau_n = \sum_{k=1}^K \frac{\omega_{nk}}{R_{nk}} \cdot \Delta\tau \quad (15)$$

where: ω_{nk} —means the number of counts in k -th sub-channel of the n -th delay cell, R_{nk} —the total number of all events registered in k -th sub-channel of n -th delay cell, $\Delta\tau$ —the ODLs resolution.

In this way, the average delay segment $\bar{\tau}_q$ can be determined by summed up all of the delay segments (within a single TDL) and divided by the number of TDL segments from following equation:

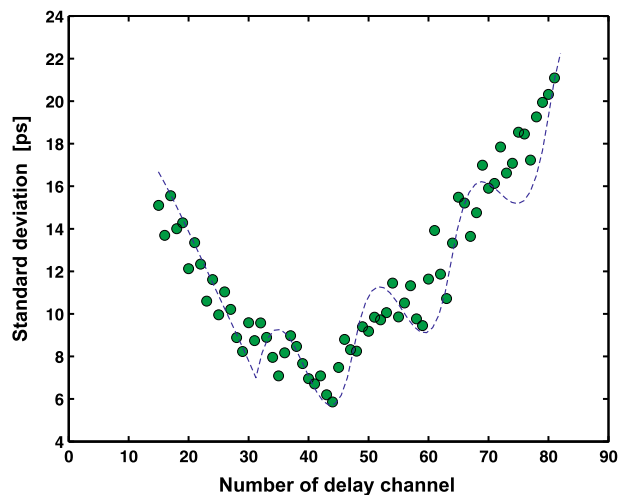
$$\bar{\tau}_q = \frac{1}{N} \sum_{n=1}^N \tau_n. \quad (16)$$

Thus, the DNL error in the n -th point of conversion characteristic is defined as the difference between width of n -th delay channel and the average value given by (16) equation:

$$DNL(n) = \frac{\tau_n}{\bar{\tau}_q} - 1. \quad (17)$$

From Eq. (17), the maximum value of DNL error in the whole measuring range is defined as follows:

Fig. 7 Multi-tap coding delay line fluctuations



$$DNL = \max_n \left\{ \left| \frac{\tau_n - \bar{\tau}_q}{\bar{\tau}_q} \right| \right\} \quad (18)$$

In this way, by summing up the various channel width deviations from the average value, the INL errors can be calculated from the following relation:

$$INL(i) = \sum_{i=\min(n)}^N DNL(i) \quad (19)$$

By analogy to DNL error, the maximum value of INL error can be obtained directly from (19) equation:

$$INL = \max_i \{|INL(i)|\} \quad (20)$$

The designated an INL error determines the information, how large an time-interval error during the measurement will be committed.

Using presented relations it was possible full characterization of TCDL. The delay cells characteristics obtained for the 200-Taps TCDL are shown in Fig. 8. The attained average quantization step was about 25 ps. Minimum and maximum quantizations were 0.1 and 67.4 ps, respectively. These results gives a wide range of delay cells variation at ± 34 ps. Whereas an example of DNL and INL characteristics obtained for the same 200-Taps TCDL are shown in Fig. 9. The presented characteristics shows a very high non-linearity. In this case, the maximum DNL and INL errors was 41.6 and 124.6 ps, respectively.

For further analysis its also reasonable to estimate the above errors for others TCDLs. The calculation results for the sixteen TCDLs are summarized in the Table 1. In reference to these informations, in Sect. 6 we explain the idea of construction an equivalent delay line (Fig. 10) as one of the methods used for improve resolution and effectively compensation of DNL and INL errors.

6 Multi-stage TCDL architecture

Unfortunately, while the TCDL resolution depends only on delay cells (DC) parameters and are characterized by a large non-linearities, the high-precision measurements is not a satisfactory solution. Typical values of individual delay elements varies in the range from several to tens of picoseconds (i.e. Virtex-4 produced on a 90 nm Copper CMOS Technology). Therefore, for further improvement of a one-shot resolution and effectively

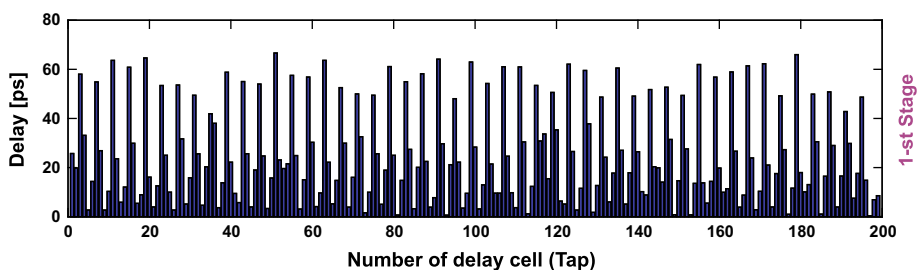


Fig. 8 The 1-st stage of 200-Taps TCDL with an 25 ps average quantization step

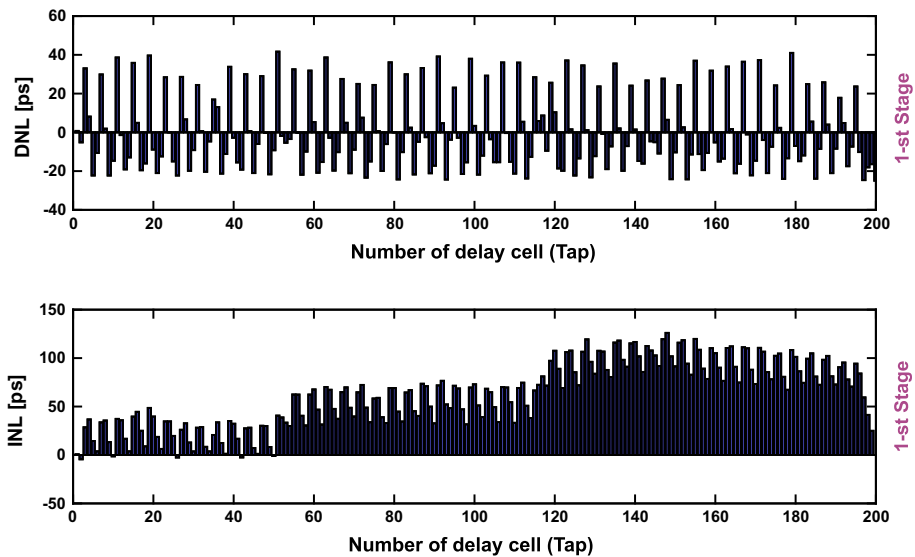


Fig. 9 Differential and integral non-linearity errors of the 1-st stage of 200-Taps TCDL

Table 1 The experimental results of DNL and INL errors for sixteen 200-Taps TCDLs with assumed $\tau_q = 25$ ps resolution

DNL (ps)							
41.55	47.94	40.90	40.97	45.29	44.96	42.86	45.30
48.37	57.36	34.69	55.93	82.52	44.86	58.91	49.72
INL (ps)							
124.57	127.24	141.59	142.61	129.19	127.06	130.81	136.07
152.54	152.71	152.95	144.30	151.23	150.87	107.84	151.95

minimization of non-linearity errors we can use the equivalent coding line (Szplet et al. 2013).

6.1 Principle of ADL and FDL realization

Improved resolution may be simply achieved by increasing the number of TCDLs and effectively parallelization of their conversion process. An application of ECDL to construction of the high-resolution TDC allows us to obtain converters with sub-gate delay time resolution. Each of these lines are composed of the specified number of TCDLs. In this case, it is very important to precisely determination of TDCLs characteristics and disturbances in the propagation times Δt_{di} (as illustrated in Fig. 10) to each of appropriate TCDLs. All of them parameters, may be obtainable by optical direct method described in Sect. 4. The propagation time values may be also determined graphically from the 2-dimensional probabilities of counts matrix as shown in Fig. 11.

Generally, we can specify two methods of the ECDL realization. The first one, concerns of ECDL realization with previously assumed resolution (ADL—assumed equivalent delay line) while the second one is a direct combination (FDL—folded equivalent delay line) of

all TCDLs. The principle of both methods, preferred to achieve a high resolution ECDL has been illustrated in Fig. 10. The presented methods allows increasing the ECDL resolution proportionally to the number of used TCDLs. For example, when we analyse the two-stage TCDL (where each of the coding delay lines contain respectively m and n quantization steps), we can obtain the converters with approximately two times better resolution. A special case of the ADL construction is the line with similar or the same resolution such as TCDLs. It explain the possibility of practical application of the first level of hardware linearization process. But we must remember that, there are cases, where a such line may not be always realized. It depends on the finite number of available (similar to the expected resolution) delay cells.

6.2 Experimental results

We achieved the various characteristics of our ECDLs. For each of ECDL realizations we using sixteen TCDLs. Their metrological parameters are summarized in the Table 1.

Firstly, we have prepared a ADL with similar resolution to TCDL (about 25 ps). The measured characteristics of the 200-Taps ADL, was shown in Fig. 12. Minimum and maximum values of quantization steps were 20.53 and 30.17 ps, respectively. The non-linearity errors have been effectively reduced to 5.16 ps. The maximal values of INL and DNL errors are less than 6 ps, which corresponds to a quarter of ADL quantization step. You will notice, that this is about seven-fold (DNL) and twenty-fold (INL) improvement in relation to results described in Sect. 5.

In the second approach, we increasing the assumed delay resolution to 10 ps and then to 5 ps. We achieved a 498 and 991 quantization steps (for the same time-interval). The INL characteristics are shown in Fig. 13. The extreme values of both non-linearities was equal to 7.74 and 18.9 ps, respectively. Minimum and maximum of quantization steps for 10 ps of ADL were 2.74 and 15.77 ps, but for 5 ps were about 0.32 and 12.91 ps. In this case, the

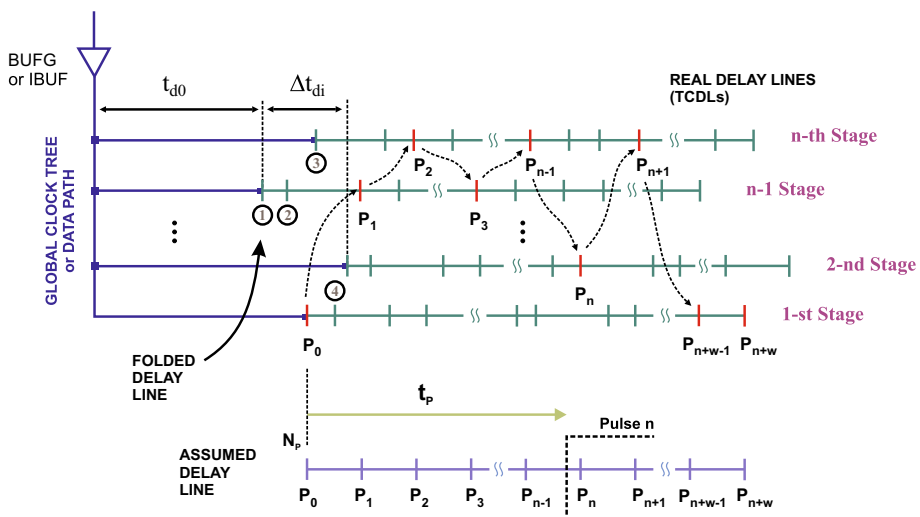


Fig. 10 Principle of the assumed and folded delay line creation (in this example we prefer the high linearity): Δt_{di} —measured differences in propagation times to each of n TCDLs stages; t_{d0} —the shortest propagation time from BUFG or IBUF buffer output to each of TCDLs inputs

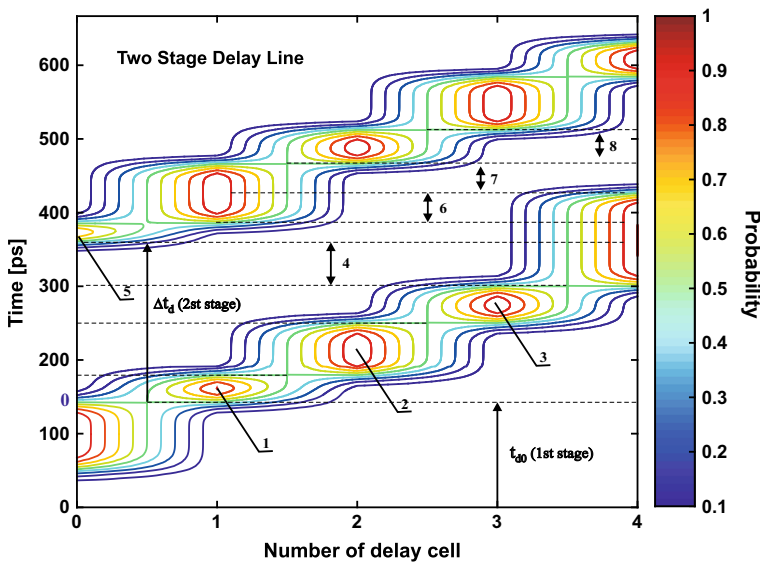


Fig. 11 Example of the multiple TCDL calibration and enumeration

extreme value of DNL errors were 7.26 and 7.86 ps, respectively. The obtained results, let us noted, that further increasing of the resolution causes the deterioration of ECDLs characteristics.

For comparative purposes, the results of the FDL characterization was also collected. The average quantization step was about 1.54 ps. The measured a extreme value of the bin width is 12.9 ps. The INL and DNL errors are shown in Fig. 14. The extreme value of INL equals to 102.69 ps, so the INL is about five times greater than for the ADL.

In summary, the best results are achieved in ADL realization with assumed 10 ps resolution. For this purpose, the DNL error is about 0.77 LSB and it is at least three times smaller than in other cases. Whereas the FDL shows a higher resolution (1.54 ps) not encountered anywhere else but characterized by a worse nonlinearities (66.7 LSB).

7 Timming accuracy analysis

Typically, precision of the TDC depends on the resolution of interpolators, its implementation architecture and reference standard clock stability described by accumulated jitter (Frankowski et al. 2011; Zieliński et al. 2009). For the small range of measured time-intervals the accumulated jitter can be omitted in the analysis. In this case, only the appropriate delay cell parameters and its deviation determines precision of time interval measurement.

Differential and integral nonlinearity characteristics of the used delay line was presented in Sect. 5.3. These measurements were performed using an optical direct method and demonstrate full compliance with a code density test method (Frankowski et al. 2015; Mota and Christiansen 1999). Using the above informations we can determine the average quantization step τ_q and quantization error. The quantization error was calculated from

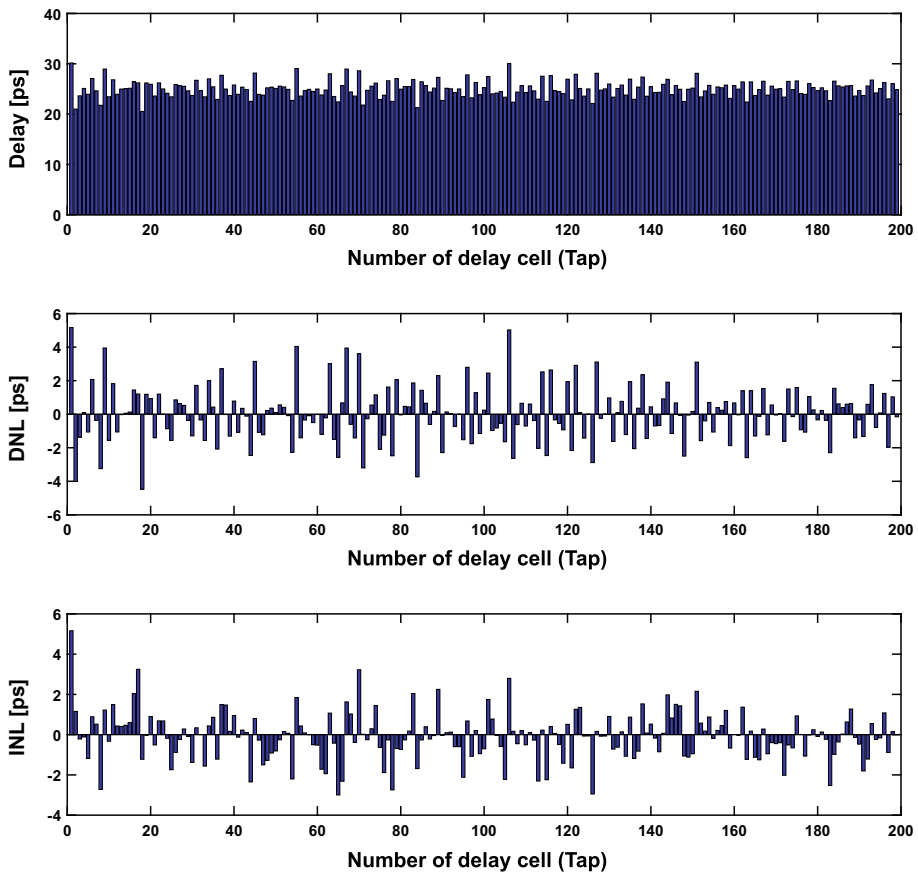


Fig. 12 An assumed equivalent delay line with a 25 ps resolution at smaller differential and integral non-linearity errors

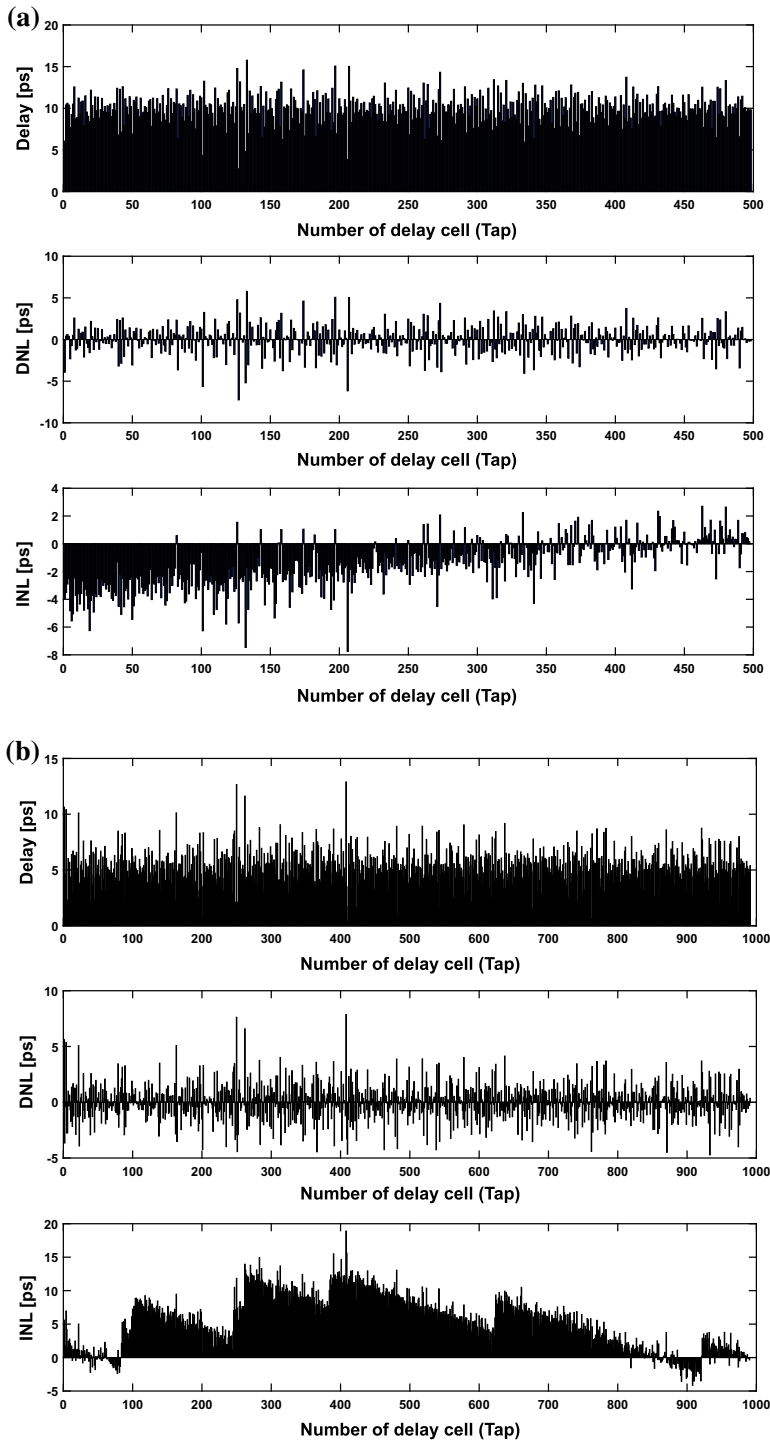
$\tau_q/\sqrt{12}$ formula and is equal 7.2 ps. Therefore, an ideal form of the quantization error distribution function can be expressed as follow:

$$\Theta_q(t) = \tau_q^{-1} p, \quad (21)$$

where p predicate assumes a one value when $-0.5\tau_q \leq t \leq 0.5\tau_q$ relation is true, otherwise the zero value. In the real case, the delay cells characteristics are not identical. Therefore, the real distribution function must be contain additional information about the deviations from the delay cells uniformity and jitter level. Hence, the distribution function $\Theta_q(t)$ is extended by an Gaussian distribution and expressed in following form:

$$\Theta_A(t, \sigma) = \int_{-\infty}^{\infty} \Theta_q(t) \Phi(t, \sigma) dt \quad (22)$$

When the phase measurement module comprises a plurality of MTDLs, then during the single conversion process it is possible to obtain many different results of time-interval measurement (depending on the number of MTDL modules). The MTDLs characteristics



◀ **Fig. 13** The ADLs characteristics obtained from the sixteen 200-Taps TCDLs: **a** the 498-Taps ADL with a 10 ps resolution, **b** the 991-Taps ADL with a 5 ps resolution

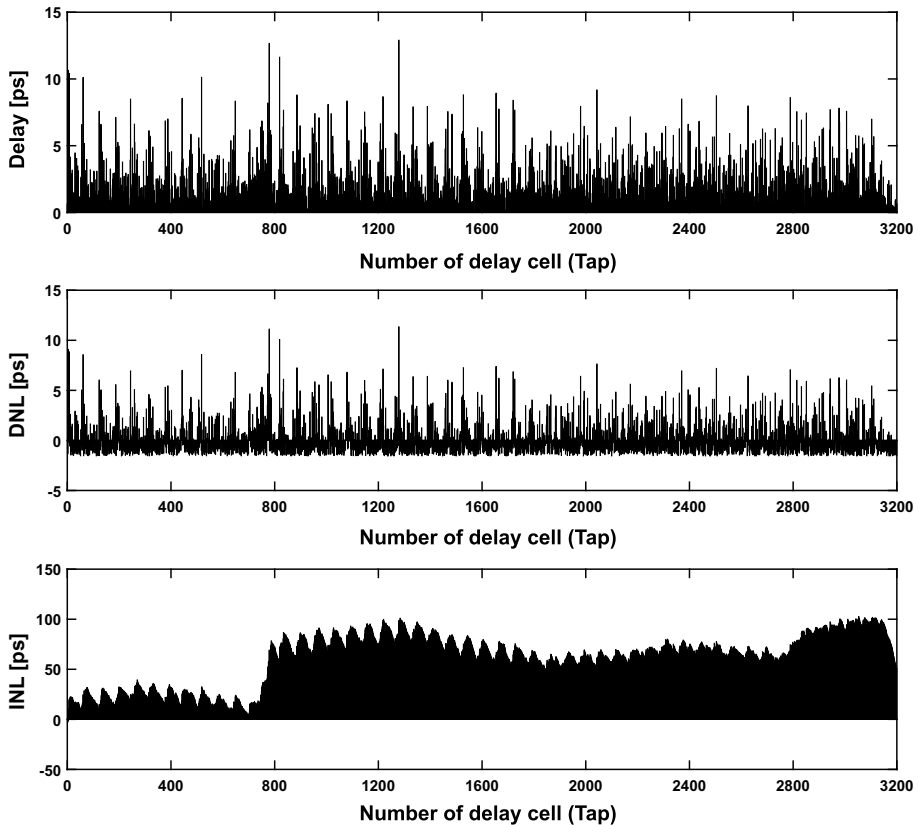


Fig. 14 The folded delay line characteristics (obtained from sixteen 200-Taps TCDLs) with a 1.54 ps quantization step

have usually different parameters. In the classical approach, each of them can be described similarly as shown for single stage TDL. Finally, it is possible to improve the system uncertainty according to the \sqrt{k} relation, where k indicates the number of delay lines. Constructed in this way delay line always requires a calibration process. Determination of the appropriate propagation times to each of delay lines with sub-picosecond resolution it is not always possible. Fortunately, using proposed in this article the ODL (as described in Sect. 4) is a good solution for this purpose. In addition to the appointed propagation times, it is also possible to obtain of the PDF for each of the newly created delay channels.

8 Examples of practical applications

Included in this paper informations may be helpful in the construction of sub-picoseconds TDCs implemented in FPGA structures. Designed and characterized (as described above) by us TDC system will be applied in different quantum physics experiments. One of

potential applications provides cooperation with an array detector of 32×32 smart pixels, where each comprising a 20- μm single-photon avalanche diode (Tisa et al. 2008). Used a high-sensitivity two-dimensional arrays of photodetectors insures a remarkable performance both in photon counting and in the photon timing measurements (Wasilewski 2008).

9 Summary and conclusions

Knowledge of the real MTDL characteristics (obtained from optical direct method) determines higher precision of the time interval measurement. Its very important solution in many fields of science, especially from the point of view on application of the high-resolution time-interval measurement system implemented in the modern reprogrammable CMOS FPGA devices.

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